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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,818	08/05/2004	Shiao-Shien Chen	14217-US-PA-X	4817

31561 7590 06/13/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/710,818	CHEN, SHIAO-SHIEN
	Examiner	Art Unit
	Long Pham	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-10 in the reply filed on 06/02/05 is acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Shokouhi et al. (US patent 6,249,458).

With respect to claim 1, AAPA teaches an electrostatic discharge (ESD) protection device, comprising (see figs. 1A-1B and 2A-2B and associated text of this application):

an ESD protection circuit, comprising:

at least a diode 112m to 112a connected in series between a first voltage V_{DD} and a pad 108; and

at least an ESD component 114a to 114n connected in series between a second voltage V_{SS} and a pad 108, wherein each of the at least an ESD component comprises a N-well region formed in a P-type substrate, and a highly doped N-type (N+) region and highly doped P-type (P+) region formed in the well region.

AAPA teaches forming the highly doped N-type (N+) region and highly doped P-type (P+) region in n N-well region that is formed in a P-type substrate but fails to teach forming the highly doped N-type (N+) region and highly doped P-type (P+) region in a triple P-well located in a deep N-well region that is formed in a P-type substrate.

Shokouhi et al. teach forming a device in a triple P-well located in a deep N-well region that is formed in a P-type substrate to limit or prevent leakage current. See fig. 7 and col. 2, lines 40-50 and col. 7, lines 45-55.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Shokouhi et al. into the structure of AAPA to prevent leakage current. See fig. 7 and col. 2, lines 40-50 and col. 7, lines 45-55.

With respect to claim 2, AAPA further teaches the N+ region of the ESD component is connected to the pad 108 and the P+ region of ESD component is connected to the second voltage. See fig. 2B of this application.

With respect to claim 3, AAPA further teaches a first ESD component and a second ESD component, the N+ region of the first ESD component is connected to the pad, the P+ region of second ESD component is connected to the second voltage V_{SS} , the P+ region of the first ESD component is connected to the N+region of the second ESD component. See fig. 1B of this application.

With respect to claim 4, AAPA further teaches a 1^{st} ESD component to the a S^{th} ESD component, the N+ region of the 1^{st} ESD component is connected to the pad, and P+ region of the last or S^{th} ESD component is connected to the second voltage V_{SS} , and the P+ region of the T^{th} ESD component is connected to the N+region of the $(N+1)^{th}$ ESD component, wherein S is a positive integer and T is positive integer from 1 to S-1. See fig. 1B of this application.

With respect to claim 5, AAPA further teaches each of at least a diode comprises a N-well region formed in a P-type substrate and a N+ region and a P+ region formed in the N-well region. See fig. 1B of this application.

With respect to claim 6, AAPA further teaches the N+region of the diode is connected to the first voltage V_{DD} and the P+ region of the diode is connected to the pad.

With respect to claim 7, AAPA further teaches a first diode and a second diode, the N+ region of a first diode is connected to the first voltage and P+ region of the second diode is connected to the pad, and the P+ region of the first diode is connected to the N+ region of the second diode. See fig. 1B of this application.

With respect to claim 8, AAPA further teaches a 1^{st} diode to a S^{th} diode, the N+ region of the 1^{st} diode is connected to the first voltage, the P+ region of the S^{th} or last diode is connected to the pad, and the P+ region of T^{th} diode is connected to the N+ region of the $(T+1)^{th}$ diode, wherein S is a positive integer and T is a positive integer from 1 to S-1. See fig. 1B of this application.

With respect to claim 9, AAPA further teaches another ESD protection circuit comprising:

a PMOS transistor 104; and

an NMOS transistor 106, wherein a gate of the PMOS transistor and a gate of the NMOS transistor are connected to the pad, a source of the PMOS transistor is connected to the drain of the PMOS transistor, a drain of the PMOS transistor is connected to the first voltage, and a source of the NMOS transistor is connected to the second voltage. see figs. 1A-1B and 2A-2B and associated text of this application.

With respect to claim 10, AAPA further teaches the ESD protection device is a radio frequency (RF) ESD protection device. see figs. 1A-1B and 2A-2B and associated text of this application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP